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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/709,729 | 05/25/2004 | Akiko F. Balchiunas | BUR920040137US1 | 3728 |

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| EXAMINER | |
|---|---|
| TANG, MINH NHUT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2829 | |

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,729 | BALCHIUNAS, AKIKO F. | |
| | Examiner | Art Unit | |
| | Minh N. Tang | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/04; 7/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statements (IDS) submitted on May 25, 2004 and July 22, 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are considered by the examiner.

### *Specification*

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means", “comprise” and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required.

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

5. Claim 22-28 are objected to because of the following informalities:

a/ in claim 22, lines 15-16, there is insufficient antecedent basis for the term "said additional failing groups". For examination purposes, "said additional failing groups" is interpreted as -- said failing groups --.

b/ claims 23-28 are objected since they depend on objected base claim.

Appropriate correction is required.

***Claim Rejections - 35 USC § 101***

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 30-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real word" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S.519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993).

A process that consists solely of the manipulation of an abstract idea is not concrete or tangible. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459. Nor can one patent "a novel and useful mathematical formula," Flook, 437 U.S. at 585, 198

USPQ at 195; electromagnetism or steam power, O'Reilly v. Morse, 56 U.S. (15 How.) 62, 113-114 (1853). **To view the new guidelines for 35 U.S.C. 101, please view the following OG notice.**

<http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm>

The claimed invention does not produce a tangible result. It is unclear how the result is being stored, displayed and used in any tangible manner.

In order to overcome the rejection, claim language should be added that includes outputting, displaying, storing or otherwise conveying the result of the previous step to be used in a tangle manner.

For examination purposes, in claim 30, lines 1-3, the limitations "A program storage ... the machine" is interpreted as -- A computer storage readable medium, tangibly embodying a program of instructions executable by a computer processor --. In claims 31-36, all in line 1, "The program storage device" is interpreted as -- The computer storage readable medium --.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Debenham (U.S.P. 5,764,650).

As to claims 1 and 30, Debenham discloses, in Figs. 1-3, a method for testing integrated circuit devices (50, 52) after manufacture, said method comprising: testing (see, for example, step 104 in Fig. 3) a group of devices (50, 52) to produce a failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed said testing (step 104), wherein said devices in said failing group (failure devices) are identified by type of failure (for example, location of bad memory cells); and retesting (see, for example, step 122 in Fig. 3) only devices in said failing group (failure devices) that have a type of defect (i.e., failures) approved for retesting.

As to claims 2 and 31, Debenham discloses in Figs. 1-3, retesting (see, for example, steps 122, 142) devices (failure devices) having types of defects (see, for example, column 1, lines 34-45) associated with testing.

As to claims 3, 10, 17, 24 and 32, Debenham discloses in Figs. 1-3, said testing process comprises probe type testing (using probes 82 shown in Fig. 2).

As to claims 4, 11, 18, 25 and 33, Debenham discloses in Figs. 1-3, said devices (50, 52) comprise integrated circuit chips (package chips and chips or dice on wafer).

As to claims 5 and 34, Debenham discloses in Figs. 1-3, said retesting process (steps 122 and/or 142) is optimized by only retesting devices in said failing group (failure devices) that have said type of defect (failures) approved for retesting.

As to claims 6, 13, 20 and 35, Debenham discloses in Figs. 1-3, a listing of types of defects (i.e., number of failures) approved for retesting comprises an optimized retest table (i.e., a record of the number of failures).

As to claims 7 and 36, Debenham discloses in Figs. 1-3, said type of defect (failures) approved for retesting is based upon previously acquired statistics of previous testing the same type of device (see column 7, lines 50-56).

As to claim 8, Debenham discloses, in Figs. 1-3, a method for testing integrated circuit devices (50, 52) after manufacture, said method comprising: testing (see, for example, step 104 in Fig. 3) an initial group of devices (50, 52) to produce an initial failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed said testing (step 104) of said initial group (50, 52), wherein said devices in said initial failing group (failure devices) are identified by type of failure (for example, location of bad memory cells); retesting (see, for example, step 122 in Fig. 3) said devices in said initial failing group (failure devices) to identify a retested passing group of devices (i.e., PASS devices) that passed said retesting (step 122); analyzing (by system controller 12) said devices in said retested passing group (PASS devices) to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure (see column 7, lines 50-58); evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting (see column 9, lines 23-30); testing (step 104) additional groups (i.e., another group of devices 50, 52) of devices (i.e., new devices 50, 52) to produce additional failing groups of devices (i.e., failure devices of new devices 50, 52, hereinafter, new failure devices) that failed said testing (step 104) of said additional groups (another group of devices 50, 52); and retesting (step 122) only devices in said additional failing

groups (new failure devices) that have one of said types of defects (failures) approved for retesting.

As to claims 9 and 16, Debenham discloses in Figs. 1-3, adding types of defects (i.e., re-identified failures) associated with testing errors (i.e., bad connection between a lead finger and a probe or other test device) to said types of defects (failures) approved for retesting.

As to claims 12 and 19, Debenham discloses in Figs. 1-3, said evaluating process optimizes said retesting (step 122) of said additional groups (another group of devices 50, 52).

As to claims 14 and 21, Debenham discloses in Figs. 1-3, said initial group of devices (50, 52) and said additional groups of devices (another group of devices 50, 52) comprise the same type of device.

As to claim 15, Debenham discloses, in Figs. 1-3, a method for testing integrated circuit devices (50, 52) after manufacture, said method comprising: testing (see, for example, step 104 in Fig. 3) an initial group of devices (50, 52) to produce an initial failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed said testing (step 104) of said initial group (50, 52), wherein said devices in said initial failing group (failure devices) are identified by type of failure (for example, location of bad memory cells); retesting (see, for example, step 122 in Fig. 3) said devices in said initial failing group (failure devices) to identify a retested passing group of devices (i.e., PASS devices) that passed said retesting (step 122); analyzing (by system controller 12) said devices in said retested

passing group (PASS devices) to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure (see column 7, lines 50-58); evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting (see column 9, lines 23-30); testing (step 104) additional groups (i.e., another group of devices 50, 52) of devices (i.e., new devices 50, 52) to produce additional failing groups of devices (i.e., failure devices of new devices 50, 52, hereinafter, new failure devices) that failed said testing (step 104) of said additional groups (another group of devices 50, 52); identifying types of devices having a predetermined reduced demand (i.e., devices for repair); and retesting (step 122) only devices in said additional failing groups (new failure devices) that have one of said types of defects (failures) approved for retesting, without retesting types of devices for which there is said predetermined reduced demand (devices for repair).

As to claim 22, Debenham discloses, in Figs. 1-3, a system (10) for testing integrated circuit devices (50, 52) after manufacture, said system (10) comprising: a tester (46) adapted to test devices (50, 52); a database (provided by the testing controller 90) comprising types of defects (for example, location of bad memory cells, failed bits, bad contacts between probes and the devices, etc.) approved for retesting, wherein said types of defects (failures) approved for retesting are based upon previously acquired statistics of which types of failures have retest passing rates, after initially failing testing, above a predetermined threshold; and a processor (12) in communication with said tester (46) and said database (90), wherein said processor

(12) is adapted to direct said tester (46) to test groups of devices (50, 52) to produce failing groups of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed the testing, wherein said processor (12) is further adapted to direct said tester (46) to retest only devices in said failing groups (failure devices) that have one of said types of defects (failures) approved for retesting.

As to claim 23, Debenham discloses in Figs. 1-3, said database (90) includes types of defects (failures) associated with testing errors (i.e., bad connection between a lead finger and a probe or other test device) within said types of defects (failures) approved for retesting.

As to claim 26, Debenham discloses in Figs. 1-3, said processor (12) optimizes said retesting of said devices (failure devices) when controlling said tester (46).

As to claim 27, Debenham discloses in Figs. 1-3, said database (90) comprises an optimized retest table (i.e., a record of the number of failures).

As to claim 28, Debenham discloses in Figs. 1-3, said statistics of said types of defects (failures) relate to the same type of device being tested.

As to claim 29, Debenham discloses, in Figs. 1-3, a system (10) for testing integrated circuit devices (50, 52) after manufacture, said system (10) comprising: means (46) for testing an initial group of devices (50, 52) to produce an initial failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices), wherein said devices in said initial failing group (failure devices) are identified by type of failure; means (46) for retesting said devices in said initial failing group (failure devices) to identify a retested passing group of devices

(PASS devices); means (12, 90) for analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure (see column 7, lines 50-58); and means (12, 90) for evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting; means (46) for testing additional groups of devices (i.e., another group of devices 50, 52) to produce additional failing groups of devices (i.e., failure devices of new devices 50, 52, hereinafter, new failure devices); and means (46) for retesting only devices in said additional failing groups (new failure devices) that have one of said types of defects (failures) approved for retesting.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

| | | |
|---|---|---|
| Stubblefield et al. | 6,043,101 | In-Situ Multiprobe Retest Method With Recovery Recognition. |
| Cirkel et al. | 2003/0062913 A1 | Testing A Batch Of Electrical Components. |
| Kobayashi | 6,728,652 | Method Of Testing Electronic Components And Testing Apparatus For Electronic Components. |
| Schuntermann et al. | 7,017,429 | Continuous Test Flow Method And Apparatus. |
| Williams et al. | 7,027,946 | Broadside Compare With Retest On Fail. |

***Communication***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Minh Tang

MINH NHUT TANG
PRIMARY EXAMINER

8/01/06